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REMARKS

Claims 21-61 are now pending.

The invention as now claimed is directed to a disk drive unit having an accessing circuit, an interface circuit, and a microcomputer. The accessing circuit is provided for accessing a disk in the disk drive. The interface circuit is coupled with a host and receives commands and/or data from the host. The microcomputer is located on a semiconductor substrate and includes a central processing unit and a nonvolatile memory. The nonvolatile memory stores programs which are executed by the central processing unit. A first program controls the accessing circuit to provide access to the disk. This first program thus controls writing and rewriting to the nonvolatile memory by the execution of other programs by the central processing unit.

Independent claims 21, 30 and 39 (corresponding to claims finally rejected in parent application Serial No. 10/023,660) require that the microcomputer check data in the nonvolatile memory by executing a second program stored in the nonvolatile memory. In response to the result of the data check, the microcomputer controls transfer of data to rewrite the first program stored in the nonvolatile memory.

According to new independent claims 42 and 52, the nonvolatile memory includes a write enabled (permission) area and a write inhibited (prohibition) area. The first program is stored in the write enabled area and the other programs are stored in the write inhibited area. The first program is capable of being written/rewritten by data received from the interface circuit via a first port, but the other programs stored in the write inhibited area cannot be written/rewritten by the data received via the first port. Instead, the other programs are written/rewritten by data received via a second port.

In the Final Rejection issued July 29, 2003 in the parent application, claims corresponding to current claims 21-41 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of U.S. Patent No. 6,393,561. The Applicants, however, believe that all of the present claims should not be subjected to a double patenting rejection over the claims of patent '561 in view of the fact that the claimed microcomputer comprises a central processing unit and a nonvolatile memory located on a semiconductor chip; the microcomputer checks data stored in the nonvolatile memory, and a first program is written/rewritten by the result of the check, and the

nonvolatile memory comprises a write enabled area and a write inhibited area, wherein the first program stored in the write enabled area can be written/rewritten by data received from an interface circuit via a first port, and the other programs stored in the write inhibited area cannot be written/rewritten by data received via the first port, but can be written/rewritten by data received via a second port.

In addition, claims corresponding to the present claims 21-41 were rejected under 35 U.S.C. §103 as being unpatentable over Horie, JP 8-30450 in view of Christeson et al, U.S. 5,579,522. Each of the current claims patentably defines over these references, whether taken individually or in combination, because the references fail to disclose that both a central processing unit and a nonvolatile memory are located on a semiconductor chip; the central processing unit checks data stored in the nonvolatile memory and a first control program written/rewritten in the nonvolatile memory based on the result of the check; and programs stored in a write inhibited area of the nonvolatile memory cannot be written/rewritten by data received by a control section, but can be written/rewritten by data received via a different port.

In particular, Horie discloses a system and scheme for updating a program in a flash memory, the system including a central processing unit 109, a ROM 111, a ROM 112, a SCSI control section 102, and transfer error detection means 115. A first control program is stored in ROM 111 and can be rewritten according to a second control program stored in ROM 112. The SCSI control section 102 receives data for rewriting the first program, and the transfer error detection means 115 detects whether errors exist in the received data for rewriting the first program.

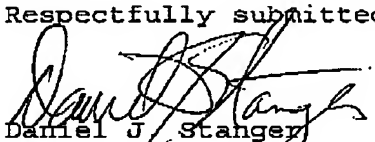
ROM 111 can be said to correspond to the claimed write enabled area, and ROM 112 can be said to correspond to the write inhibited area. However, ROM 112 is a mask ROM, and thus cannot be rewritten, whereas the claimed write inhibited area can be rewritten by data received via the claimed second port. Alternatively, Horie teaches that the two ROMs 111, 112 can be located in a single flash memory, wherein ROM 112 is arranged to be a non re-writable boot block.

Christeson is cited as teaching a program that checks data in an electronically erasable programmable nonvolatile memory. However, Christeson does not teach the features noted above which are missing from Horie, and the person of ordinary skill is provided with no motivation to modify Horie simply to

provide a check of data. Even if so modified, the resulting combination would not satisfy all the requirements of the claims as noted above.

In view of the foregoing amendments, new claims, and remarks, the Applicants submit that the application is free of the prior art represented by Horie and Christeson, whether taken individually or in combination. Therefore, the Applicants request reconsideration of the prior Final Rejection and allowance of the claims.

Respectfully submitted,



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